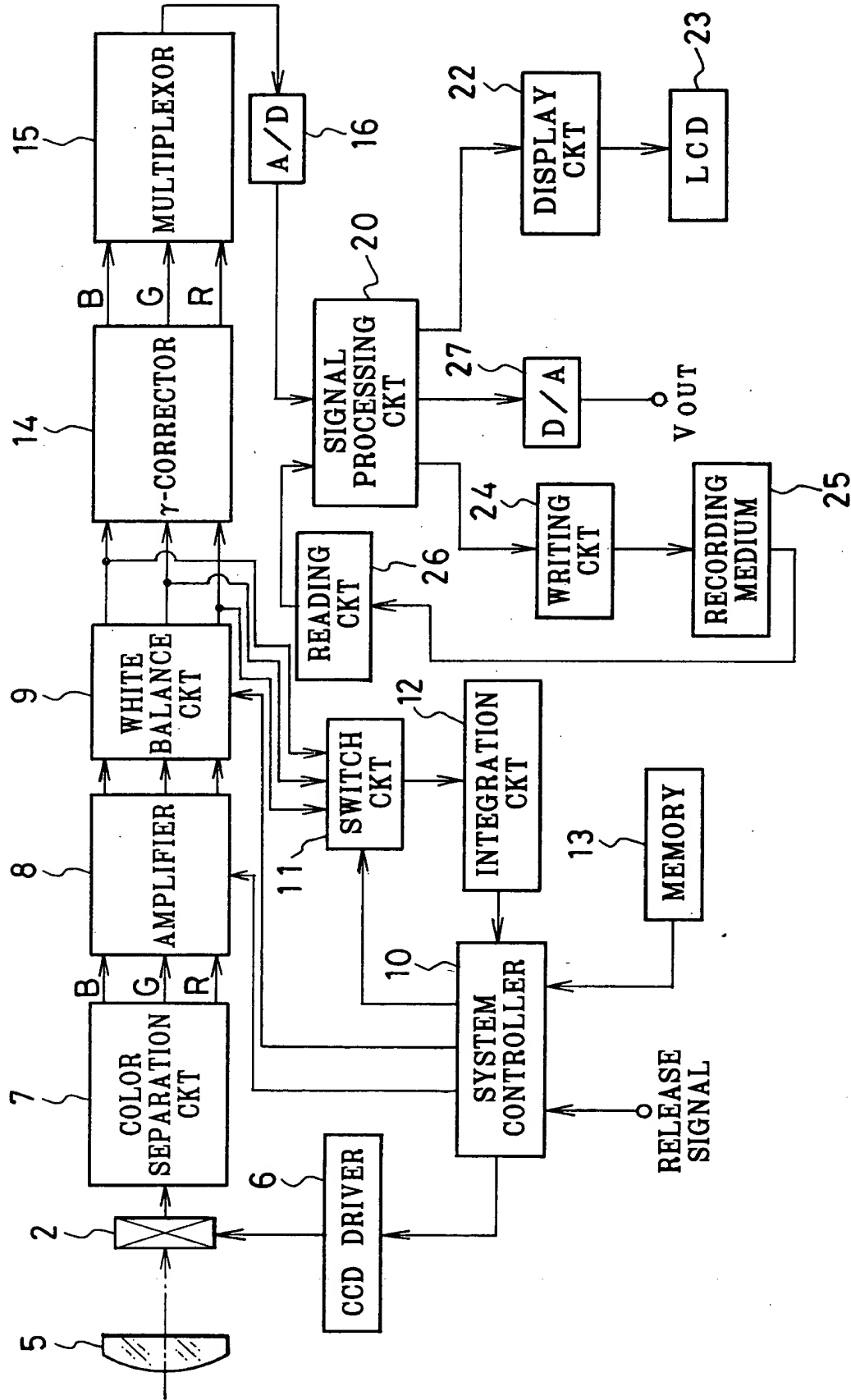
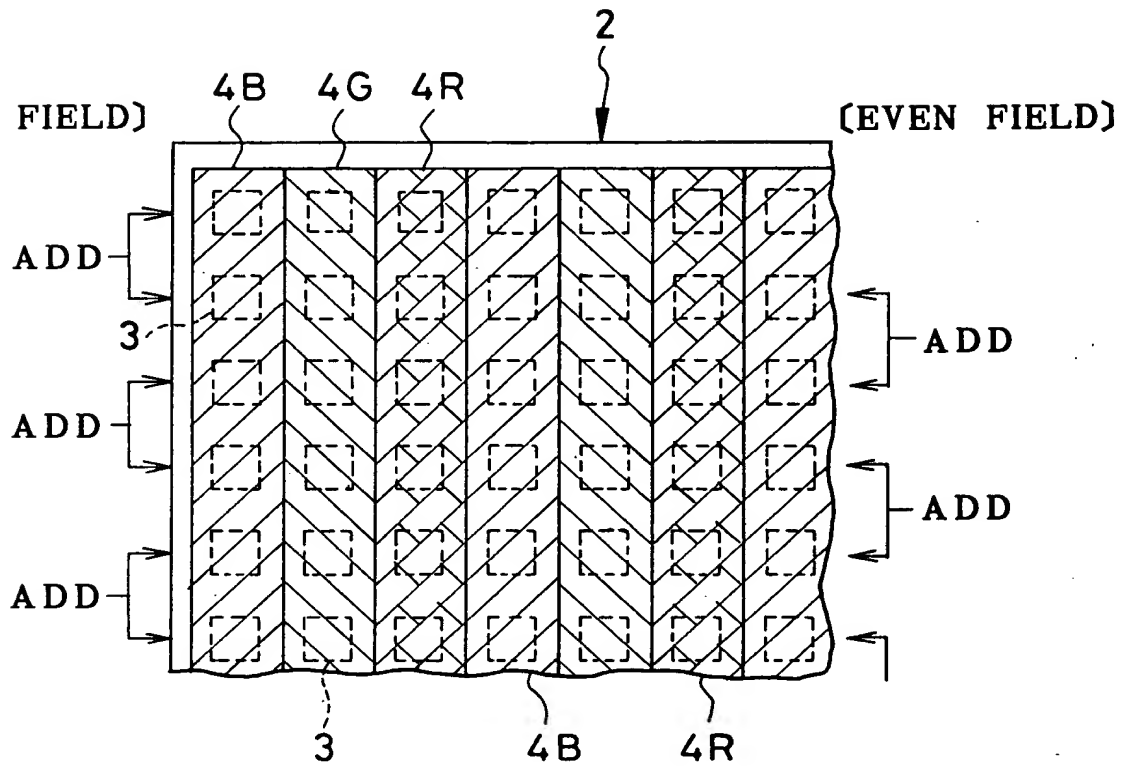


FIG. 1



The diagram illustrates a color filter structure for odd and even fields. It shows a grid of subpixels arranged in columns labeled 4B, 4G, and 4R. The structure is divided into two main sections: [ODD FIELD] on the left and [EVEN FIELD] on the right. A central vertical line is labeled 2. The grid is composed of a series of vertical lines, with the space between them labeled 3. The subpixels are represented by dashed squares, and the entire structure is overlaid with a series of diagonal lines. Brackets labeled ADD are shown on both the left and right sides, indicating the addition of light or signal. The bottom of the diagram is labeled 3, 4B, and 4R.



The diagram illustrates the timing sequence for the image pickup system. It consists of six horizontal tracks:

- SHUTTER RELEASE:** A single pulse at the beginning of the sequence.
- VSYNC:** A series of vertical sync pulses. The first three pulses are labeled with a time interval  $T_1$ , and the subsequent two are labeled with a time interval  $T_2$ .
- CHARGE STORAGE TIME:** A signal that is high during the  $T_1$  intervals and low during the  $T_2$  intervals.
- CCD OUT:** A signal that is high during the  $T_1$  intervals and low during the  $T_2$  intervals. Arrows point from the first three high pulses to the LCD signal and from the fourth high pulse to the Image Signal Recording signal.
- LCD:** A signal that is high during the  $T_1$  intervals and low during the  $T_2$  intervals. Arrows point from the first three high pulses to the CCD OUT signal and from the fourth high pulse to the Image Signal Recording signal.
- IMAGE SIGNAL RECORDING:** A signal that is high during the  $T_2$  intervals and low during the  $T_1$  intervals. An arrow points from the fourth high pulse to the CCD OUT signal.

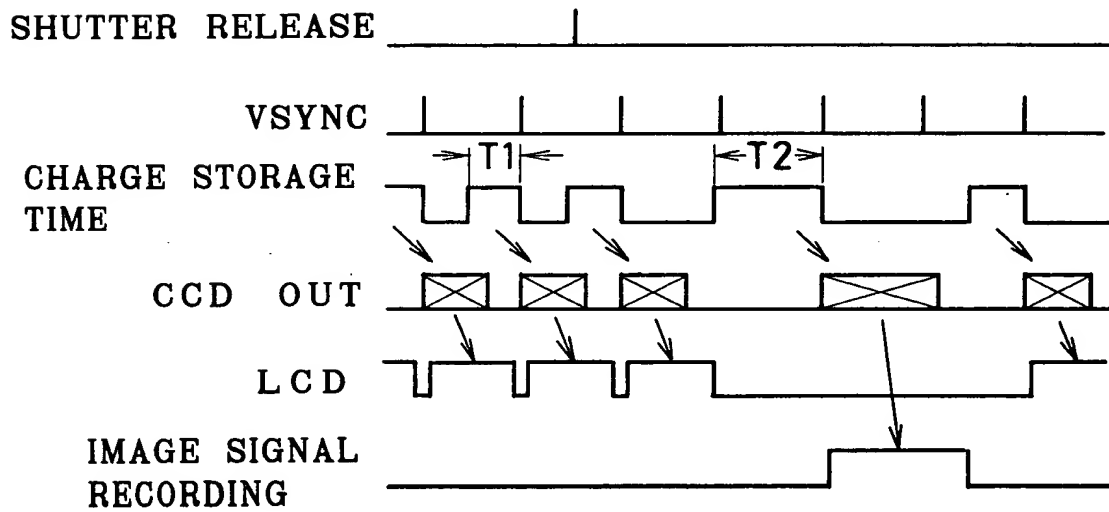


FIG. 4

